

APPLICATION  
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Applicant

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For

"COPPER TO ALUMINUM INTERLAYER  
INTERCONNECT USING STUD AND VIA LINER"

Docket

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COPPER TO ALUMINUM INTERLAYER INTERCONNECT  
USING STUD AND VIA LINER

DESCRIPTION

BACKGROUND OF THE INVENTION

5 Field of the Invention

10 The present invention generally relates to semiconductor integrated circuit chips and packages therefor and, more particularly, to interlayer interconnects and fine pitch intralevel interconnects in the connection pad layer in semiconductor integrated circuits and packages therefor.

Description of the Prior Art

15 Extremely high integration density has been pursued in recent years due to the increases in performance due to reduced signal propagation time as well as increased functionality and increased economy of manufacture. Nevertheless, integrated circuit complexity is primarily limited by the  
20 ability to make a sufficient number of power and signal connections to and from a given chip to a package and vice-versa. The same limitation applies to the interface of the package and the board or device in which the package is included. Since a  
25 chip of sufficient complexity to require only power, data and control inputs and outputs (e.g. a system-

on-a-chip) is not generally available at the present time (except as relatively simple application specific integrated circuits (ASICs)), many hundreds if not thousands of connections between a chip and its packaging are generally required. Numerous wire bonding and solder preform techniques (e.g. C4) are well-known for making such numerous and closely spaced connections with high reliability.

However, to increase signal propagation speed and enhance the effects of extremely high integration density, the use of copper wiring interconnects on the chip and in packaging has become the metallurgy of choice for high performance devices. At the same time, aluminum metallurgy is preferred for final interconnect and so-called distribution layer interconnections due to the ability of forming extremely fine interconnects at fine pitch and in close proximity with each other where the interconnects can be encapsulated to eliminate significant metal migration. Further, aluminum metallurgy is preferred for chip and package solder and wire bonding connection pads. Wire bond and C4 solder connections are considered to require a last metal connection pad layer of aluminum due to, at least, the solubility of copper in solder materials and other metals causing the development of undesired structures or damaging effects as copper precipitates upon cooling.

To integrate aluminum wiring and pad metal levels with lower copper wiring metal layers, it has been necessary to form large copper plugs or pads overlaid by a large aluminum via and a large

aluminum pad to make connections to aluminum layers. However, such a large pad effectively prevents interconnection wiring from being provided in the same aluminum layer, at least in the numbers and complexity of interconnections generally required for many integrated circuits at the present time.

For connection between aluminum wiring and/or pad levels, vias much smaller than the copper and aluminum pad and via interface structures can be used. Tungsten has become a metal of choice for such vias or studs between aluminum metallurgy layers and suitable tungsten via/stud formation processes are well-known. Tungsten studs have generally been used for their low resistivity, good reliability and good adhesion to aluminum. However, tungsten fluoride ( $WF_6$ ) must be used for chemical vapor deposition processes to deposit the tungsten studs in vias of the chip or package.

Unfortunately, tungsten fluoride tends to attack copper causing corrosion and some potentially significant and uncontrolled etching of the copper. This effect can unpredictably cause reduction in manufacturing yield and/or variation of device electrical properties. Certainly, processes which allow for uncontrolled chemical processes to take place will not support foreseeable increases in integration density and smaller sizes and finer pitches of copper connections. For this and other possible reasons, tungsten studs have not been used to connect to copper

It should be understood that the formation of a metal layer is a time-consuming process; adversely

affecting tool throughput and productivity.

Further, there is a large economic cost associated with the duration of such processes and tool and facility amortization represents a substantial

5 fraction of device cost. These problems are aggravated by the fact that copper processes, per level, are more time-consuming than aluminum layer processes for suitable interconnects made below the copper to aluminum interface structure layer.

10 Moreover, it should be recognized that the copper to aluminum interface structures require essentially the same pattern to be formed in two separate metal layers which, together, have the sole function of altering metallurgy to accommodate solder and wire  
15 bonding connections at yet another metal layer level.

This cost of copper processes may be well-justified at lower interconnect layers where signals are being communicated between active devices on the  
20 chip and where critical paths are much more likely to exist for correct functioning of the overall integrated circuit. However, once the full functionality of the chip has been achieved, leading signals on and off the chip is much less critical  
25 and the additional delay is generally small relative to the overall path length to be traversed between chips. By the same token, the processing time required for provision of a copper wiring layer (for optimum device performance), together with an  
30 aluminum layer represents a significant portion of the total wafer processing time for a state of the art, high density integrated circuit chip or wafer.

Therefore, the costs per chip of known structures for integration of copper and aluminum may be substantial for each chip but have been unavoidable when performance requirements have left no alternative to integration of copper and aluminum.

## SUMMARY OF THE INVENTION

It is therefore an object of the present invention to provide a technique of integrating copper and aluminum utilizing tungsten studs which avoids attack of the copper by the tungsten deposition process.

It is another object of the invention to provide for integration of copper and aluminum wiring in an integrated circuit chip utilizing a single aluminum layer for both connection pads and interconnect wiring.

In order to accomplish these and other objects of the invention, an integrated circuit is provided including a patterned copper layer, a patterned aluminum layer, a stud connection in an opening between the patterned copper layer and the aluminum layer, and a liner in the opening and extending between the stud and the patterned copper layer.

In accordance with another aspect of the invention, a method of forming an interface structure between copper and aluminum metallurgy layers in an integrated circuit is provided comprising steps of covering a copper metallurgy layer with an insulator, forming an opening through the insulator to the copper metallurgy layer, forming a liner of a conductive barrier material in the opening, filling a remainder of the opening with a conductive material to form a stud, and forming a patterned aluminum metallurgy layer over the stud.

## BRIEF DESCRIPTION OF THE DRAWINGS

The foregoing and other objects, aspects and advantages will be better understood from the following detailed description of a preferred embodiment of the invention with reference to the drawings, in which:

Figure 1 is a cross-sectional view of a first, generalized embodiment of the invention, and

Figure 2 is a cross-sectional view of a preferred embodiment of the invention.



DETAILED DESCRIPTION OF A PREFERRED  
EMBODIMENT OF THE INVENTION

Referring now to the drawings, and more particularly to Figure 1, there is shown, in cross-section, a generalized embodiment 10 of the present invention illustrating the basic principles thereof. It should be understood that Figure 1 includes only the uppermost copper metal levels of an integrated circuit device of largely arbitrary design. That is, the integrated circuit device below the level indicated by angled arrow 20 is formed by a process of record including copper interconnects and the design, layout and collective function of the active or passive devices (exemplified by fuse 15) of the integrated circuit below this level are not important to the practice of the invention.

However, it should be clearly understood that while a portion of the structure illustrated in Figure 1 and 2 is formed by a process of record and does not directly include the invention, no portion of Figure 1 or 2 is admitted to be prior art as to the present invention. On the contrary, entire integrated circuits and/or packaging therefor obtain unexpected advantages from inclusion of the invention and thus similarly embody the invention.

This integrated circuit structure is covered with a barrier layer 25 such as nitride which prevents diffusion of contaminants such as oxygen from higher levels or even the environment of the chip. The nitride barrier layer is then covered with an insulator layer 35 of, for example, oxide,

low dielectric constant (low-k) material or the like as may be desired or required by the electrical characteristics necessitated by the design. The low-k material and the barrier layer are then  
5 patterned to open the insulator and nitride layer where connections are to be made. However, in accordance with the invention, the opening need not be large as in known copper to aluminum interface structures but can be dimensioned in accordance with  
10 known via/stud structures.

This via/stud opening is then lined with a conductive material which can also serve as a barrier to reactant materials such as tungsten fluoride which will be used in subsequent processes.  
15 The material forming liner 40 can be any material or combination of materials such as layers of titanium and titanium nitride or PVD tungsten which has low electrical resistivity, good adhesion to both copper and tungsten as well as to oxide and good barrier  
20 properties against interdiffusion of copper and tungsten (or other stud material) and tungsten fluoride attack. Any substantially isotropic deposition or growth process is suitable for formation of liner 40.

The via/stud opening thus lined with liner 40 can then be filled with metal, preferably tungsten, to form stud 50 and covered with a layer 60 of, preferably, a titanium nitride adhesion layer and an aluminum metal layer 65 which can then be patterned  
30 as desired. to form interconnection wiring and/or solder or wire bond pads. Freedom of design in such patterning is supported by the small via/stud area

40, 50 which is much smaller than the aluminum via previously known for integration of copper and aluminum. Therefore, features patterned in the first aluminum layer can be comparable in size to features in any copper layer and both connection pads and interconnect wiring can thus be included within the same aluminum layer. Doing so allows not only elimination of an aluminum layer but permits interconnect wiring to be performed in an aluminum layer with substantial process time reduction compared to a copper interconnect layer.

sub c1 The device is then completed by provision of suitable insulating, passivation and/or protective layers, preferably in a sequence of layer 80 of TEOS oxide (or, preferably, a silane-based high density plasma oxide), a nitride layer 90 and a polyimide layer 100 which may be photosensitive or not, as desired. A photosensitive polyimide is often preferred, however, when aluminum wiring level 65 includes solder or wire bond pads 105, as shown in Figure 1. a further titanium nitride layer 70 can also be placed over the aluminum features 65, if desired for enhancement of adhesion to layer 80 or otherwise provide protection or enhancement of conduction characteristics of aluminum features but may be removed in the solder or wire bond areas.

Referring now to Figure 2, a preferred form of the invention and a preferred process for its fabrication will now be discussed in detail. It should be appreciated that the structure illustrated in Figure 2 is very similar to that of Figure 1 except that aluminum wiring 65 remains covered by

titanium nitride 70 and layers 80, 90 and 100 since a solder or wire bond pad is not formed in the particular location of the cross-section of Figure 2 (thus illustrating that both can be formed in the same layer) and that the liner 40 in the via stud opening is preferably formed of tantalum nitride 110 followed by a liner layer 120 of tungsten, preferably deposited by a PVD process, which assists in proper formation of the tungsten stud 50.

Once the integrated circuit design has been formed and the barrier (e.g. nitride) layer 25 formed, an insulator layer 35 of a material supporting the formation of Damascene vias is applied. Many suitable materials such as oxides and low-k materials are known to those skilled in the art. The insulator and barrier layers 35, 25 are preferably opened using a reactive ion etch (RIE) to form via openings 30.

Tantalum nitride liner 110 is preferably formed by a PVD process using DC target power of between about 0.5 and 4.0 KW, an argon gas flow of between about 20 and 150 Sccm and a nitrogen gas flow of between about 10 and 81 Sccm corresponding to pressures between about 1.0 and 10.0 mTorr. Ionized PVD having similar DC power, RF coil power between about 0.5 to 4.0 KW and wafer bias power ranging from zero to 450 Watts, argon gas flow of about 10 and 150 Sccm and nitrogen gas flow of about 10 to 80 Sccm corresponding to pressures of between about 1.0 and 40.0 mTorr can also be used. Such a process favors deposition on horizontal surfaces to deposition on vertical surfaces and is preferably

carried out to a thickness of between 10 and 200 Angstroms at the bottom of the via/stud opening and between about 10 to 100 Angstroms on the sides.

Deposition of tungsten layer 120 is preferably performed to a similar thickness by a PVD or ionized PVD process under similar conditions to those used for tantalum nitride. The remainder of the via/studs opening can then be filled with tungsten by any known process and the tungsten polished back to the surface of insulator 35. A thin polish stop of, for example, nitride, can be used to facilitate this process, if desired. The aluminum layer 65 (preceded and/or followed by titanium and/or titanium nitride to form a stack structure, if desired) can then be formed and patterned and the device completed as discussed above.

In view of the foregoing, it is seen that the invention provides a copper to aluminum interface structure which allows interconnections and/or solder or wire bond pads to be formed in the same layer, allowing substitution of a layer of aluminum interconnects for a layer of copper interconnects. These simplifications of integrated circuit structure improve performance and significantly reduce fabrication time and increase tool throughput; thus reducing integrated circuit costs. These meritorious effects are achieved while avoiding deleterious effects of process materials on copper which can compromise performance and/or reliability of the integrated circuit.

While the invention has been described in terms of a single preferred embodiment, those skilled in

the art will recognize that the invention can be practiced with modification within the spirit and scope of the appended claims.

FOR RELEASE